



Drafts

Pending

Active

- ✓ L1: (8) (((temporal adj5 logic) and (state adj3 machine) and (condition\$3 near9 transition\$4)) and (state near9 test\$4)) near9 operat\$4
- ✓ L3: (7) 11 and 12
- ✓ L4: (54126) state near9 test\$4
- ✓ L2: (71001) event near9 operat\$4
- ✓ L5: (1) 13 and 14
- ✓ L6: (115294) (event or tempora\$3 or logic or transit\$4 or state or count\$4) near9 test\$4
- ✓ L7: (7) 13 and 16
- ✓ L8: (1) 6581191.pn. and 16

Failed

Saved

	U	I	Document ID	Title	Count
1	<input type="checkbox"/>	<input type="checkbox"/>	US 20040025122	Hardware-based HDL code coverage and design analysis	71
2	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20030182642	Hardware debugging in a hardware description language	71
3	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20030131325	Method and user interface for debugging an electronic system	71
4	<input type="checkbox"/>	<input type="checkbox"/>	US 20030069724	Method and system for debugging an electronic system using instrument	70
5	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20030046658	Event-based temporal logic	71
6	<input type="checkbox"/>	<input type="checkbox"/>	US 6618839 B	Method and system for providing an electronic system design with enha	71
7	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6581191 B1	Hardware debugging in a hardware description language	71

Details

HTML

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Help